BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

(19) Europäisches Patentamt
European Patent Offic
Office européen des brev ts

(11) Publication number: **0 062 431**
A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 82301445.1

(22) Date of filing: 19.03.82

(51) Int. Cl.³: G 06 F 3/04, G 06 F 15/06

(30) Priority: 20.03.81 JP 40801/81
25.03.81 JP 43503/81

(43) Date of publication of application: 13.10.82
Bulletin 82/41

(84) Designated Contracting States: DE FR GB NL

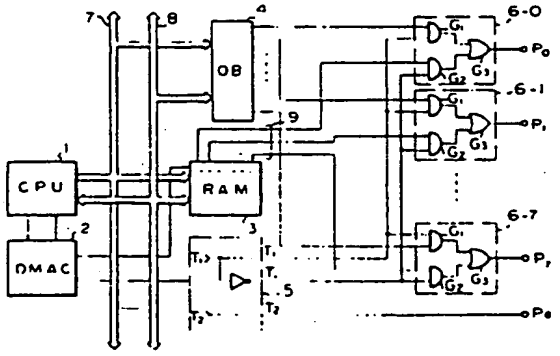
(71) Applicant: FUJITSU LIMITED, 1015, Kamikodanaka Nakahara-ku, Kawasaki-shi Kanagawa 211 (JP)

(72) Inventor: Murakami, Jyoji, 236-1-410 Suwa Takatsu-ku, Kawasaki-shi Kanagawa 213 (JP)
Inventor: Watanabe, Tsuyoshi, 568-9, Higashihongo-cho Midori-ku, Yokohama-shi Kanagawa 226 (JP)

(74) Representative: Reckham, Stephen Neil et al, GILL JENNINGS & EVERY 53/64 Chancery Lane, London WC2A 1HN (GB)

(54) A one chip microcomputer.

(57) A one ship microcomputer comprises:
a central processing unit (CPU 1) having arithmetic, logic and control units; a random access memory (RAM 3) for storing intermediate data with instructions processed by the central processing unit (CPU 1); means (4, 23) for carrying first data processed by the central processing unit (CPU 1); a direct memory access controller (DMAC 2) controlled by the central processing unit (CPU 1) for providing a read out of second data stored in a predetermined area of the random access memory (RAM 3); means (9, 21) for carrying the second data stored in the predetermined area of the random access memory (RAM 3); terminal means (P) coupled to said means for carrying the first and second data to provide an output for the first data during a central processing unit operating mode and for the second data during a direct memory access operating mode; and, a time division means (5) controlled by the direct memory access controller (DMAC 2) for transmitting the first or the second data to the terminal means (P). This has the advantage that a direct transfer can take place between the RAM 3 and the outside without the provision of any additional terminals.



EP 0 062 431 A1

A ONE CHIP MICROCOMPUTER

The present invention relates to a one chip microcomputer.

In the early seventies, a 4-bit microprocessor such as an Intel 4004, which was also called a microcomputer only had a central processing unit (abbreviated CPU) formed on a single chip. In recent years, however, LSI (Large Scale Integration) technology has developed with the result that highly-integrated one chip microcomputers have been also developed. A one chip microcomputer generally comprises a CPU, a random access memory (abbreviated RAM), a read only memory (abbreviated ROM), input/output (abbreviated I/O) ports, a clock generator and the like all formed on the same single chip. In other words, such a one chip microcomputer has all the computer functions on a single chip and, accordingly, its cost-performance is greatly enhanced.

In conventional one chip microcomputers, since the CPU and the RAM are connected by interconnections within a chip, data transfer therebetween cannot generally be monitored from the outside. As a result, it is difficult to test the chip to detect any malfunctions in it. Therefore, it is necessary to transfer data from the RAM to the outside or vice versa, to be able to monitor the CPU operation state.

Several approaches may be taken to meet this requirement for one chip microcomputers. One approach is to cause the CPU to perform the data transfer between the RAM and the outside. In this case, however, the load on the CPU becomes large and, accordingly, the throughput

of the microcomputer is reduced. In addition, instruction sequences (programs) are fixed in the ROM and, therefore, the operation state of the CPU is unclear. As a result, it is difficult to access a desired area of the RAM by the CPU. Another approach is to use direct memory access (abbreviated DMA). That is, under the control of a direct memory access controller (abbreviated DMAC), which is set by the CPU, a direct transfer of data is provided between the RAM and the I/O ports. In this case, however, I/O ports specifically for the DMA operation mode are necessary, and thus the number of terminals (pins) connected to the I/O ports is therefore increased. For example, in the case of an 8-bit parallel transfer system, eight additional terminals are necessary, which is disadvantageous in practice. In addition, such additional terminals are generally necessary only during the manufacture and testing of the microcomputer and, thereafter are redundant.

It is, therefore a principal object of the present invention to provide a one chip microcomputer which is able to provide direct data transfer between its RAM and the outside and yet which has only the minimum number of I/O ports.

According to the present invention a one chip microcomputer comprises:

a central processing unit having arithmetic, logic and control units;

a random access memory for storing intermediate data with instructions processed by the central processing unit;

means for carrying first data processed by the central processing unit;

a direct memory access controller controlled by the central processing unit for providing a read out of second data stored in a predetermined area of the

random access memory;

means for carrying the second data stored in the predetermined area of the random access memory;

terminal means coupled to said means for carrying the first and second data to provide an output for the first data during a central processing unit operating mode and for the second data during a direct memory access operating mode; and,

a time division means controlled by the direct memory access controller for transmitting the first or the second data to the terminal means.

The means for carrying first data processed by the central processing unit may comprise an output buffer register for storing the first data, and the means for carrying the second data may be a port means for receiving both the first data from the output buffer register and the second data from a predetermined area of the random access memory.

Alternatively, the means for carrying first data processed by the central processing unit may comprise an output buffer register for storing the first data, and the means for carrying the second data may be a gate means controlled by the central processing unit, an address port means for transmitting an externally applied address signal to the random access memory under the control of the gate means so as to read the second data from the random access memory and port means for receiving the first data from the output buffer register and the second data from the random access memory when read by the address port means.

The means for carrying the first data may also be formed by a register which is arranged to store the same data as is stored in a predetermined area of the random access memory, the write operation upon the register and upon said predetermined area of the random access

memory being performed simultaneously by the central processing unit, and in this case the means for carrying the second data is a parallel-serial converter means controlled by the central processing unit for converting parallel data into serial data, the parallel data being sent from the register by the direct memory access controller.

Finally, the means for carrying the first and second data may be formed by a parallel-serial converter means controlled by the central processing unit, for converting parallel data into serial data, and in this case, the microcomputer includes an address counter controlled by the direct memory access controller for generating an address signal to read the second data from the random access memory.

Various embodiments of the present invention will now be described with reference to the accompanying drawings; in which:-

Figure 1 is a block diagram of a first embodiment;

Figures 2A and 2B are timing diagrams illustrating signals generated in the first embodiment;

Figure 3 is a block diagram of a second embodiment;

Figures 4A to 4C are timing diagrams illustrating signals generated in the second embodiment;

Figure 5 is a block diagram of a third embodiment;

Figures 6A to 6J are timing diagrams illustrating signals generated in the third embodiment;

Figure 7 is a block diagram of a fourth embodiment; and,

Figure 8 is a block diagram of a fifth embodiment.

In Figure 1, which illustrates a first embodiment of the one chip microcopputer according to the present invention, 1 is a central processing unit (CPU) having arithmetic, logic and control units; 2 is a direct memory access controller (DMAC) which is set by the CPU 1; 3 is a random access

memory (RAM) for storing intermediate data and instructions processed by the CPU 1; 4 is a output buffer register for storing output data processed by the CPU 1; 5 is a time--division control circuit controlled by the DMAC 2; 6-0, 6-1, ..., 6-7 are I/O ports; 7 is a data bus; and 8 is an address bus. The RAM 3 has a data bus 9 for the direct memory access (DMA) operation mode. All the elements of Fig. 1 are formed on a single semiconductor chip.

During the CPU operation mode, output data (which is referred to as CPU output data) is stored in the output buffer register 4 and, after that, the CPU output data is transferred through the ports 6-0, 6-1, ..., 6-7 and terminals P_0 , P_1 , ..., P_7 to the exterior. Contrary to this, during the DMA operation, output data (which is referred to as DMA output data) is read out of a predetermined area of the RAM 3 to the DMA data bus 9 by the DMAC 2. In this case, the predetermined area is comprised of one word or eight bits. The DMA output data is also transferred through the ports 6-0, 6-1, ..., 6-7 and the terminals P_0 , P_1 , ..., P_7 to the exterior. Time-division control for such two kinds of output data is performed by the time-division control circuit 5 which is also controlled by the DMAC 2.

In more detail, the time-division control circuit 5, which is controlled by the DMAC 2, generates a clock signal T_1 as illustrated in Fig. 2A, its inverted signal $\overline{T_1}$ and a clock signal T_2 as illustrated in Fig. 2B. In this case, the difference in phase between the clock signals T_1 and T_2 is about 90 degrees. Such clock signals T_1 and T_2 can be easily formed by using a reference signal of a reference clock generator and frequency dividers (not shown). On the other hand, each of the ports 6-0, 6-1, ..., 6-7 comprises two AND gate G_1 and G_2 , and an OR gate G_3. Each gate G_1 transmits the CPU output data from the output buffer register 4 to the exterior when the potential of the clock signal T_1 is high, while each gate G_2 transmits the DMA output data from the RAM 3 to the exterior when the potential of the clock signal $\overline{T_1}$ is high. Thus, the CPU output data

and the DMA output data are alternately transmitted through the ports 6-0, 6-1, ..., 6-7 and the terminals P_0, P_1, ..., P_7 to the exterior.

It should be noted that the read operation timing of the DMAC 2 for the RAM 3 is in synchronization with the high potential of the clock signal $\overline{T_1}$.

Next, the separation of the CPU data and the DMA data will be explained. In an external circuit (not shown), when the data at the terminals P_0 through P_7 is read by the fall of the potential of the clock signal T_2 from the terminal P_8, the CPU output data is obtained. Contrary to this, when the data at the terminals P_0 through P_7 is read by the rise of the potential of the clock signal T_2, the DMA output data is obtained.

Fig. 3 is a block diagram illustrating a second embodiment of the one-chip microcomputer according to the present invention. In Fig. 3, an address counter 10, an address bus 11, an OR gate 12 and a NOR gate 13 are added to Fig. 1. In addition, the time-division control circuit 5 generates an inverted signal $\overline{T_2}$ of the clock signal T_2 to a terminal P_9. The DMAC 2 increases the address counter 10 which generates an address signal to the DMA address bus 11. Therefore, a plurality of words which serve as the DMA data are read out of the RAM 3 to the DMA data bus 9. For example, if the address counter 10 comprises 4 bits, eight words allocated by addresses "0", "1", "2", ..., "7" can be read out from the RAM 3.

The CPU data and the DMA data are alternately transmitted through the ports 6-0, 6-1, ..., 6-7 to the terminals P_0, P_1, ..., P_7, in the same way as in Fig. 1. In this case, however, it is necessary to know the address of a DMA output data (word) transmitted at the terminals P_0, P_1, ..., P_7. For this purpose, a terminal P_9 is provided.

The output potential of the OR gate 12 is low only when the value of the address counter 10 is 00 ... 0(="0"). In addition, as illustrated in Figs. 4A, 4B and 4C, the output potential T_3 of the NOR gate 13 is high only when the

potential of each of the signals T_1 and $\overline{T_2}$ and the value of the address counter 10 is "0". Therefore, the value of the address counter 10 can be read by providing an appropriate external counter (not shown). That is, the external counter is reset by the rise of the potential T_3 at the terminal P_9 and increases one count by the rise of the potential T_2.

Fig. 5 is a block diagram illustrating a third embodiment of the one-chip microcomputer according to the present invention. In Fig. 5, terminals P_{11} through P_{19}, an address port 14 and gates G_{11} through G_{19} are provided so as to access the RAM 3 directly from the exterior during the DMA operation mode. Each of the ports 6-0, 6-1, ..., 6-7, which comprises six gates G_1 through G_6, is bidirectional. The bidirectional I/O ports 6-0, 6-1, ..., 6-7 are connected to a DMA write data bus 15. D-type flip-flops 16 and 17, and an AND gate 18 are provided for a permission signal T_7, which permits a DMA read or write operation.

In more detail, by the rise of the potential of the signal T_1, as illustrated in Fig. 6A, the flip-flop 16 takes in the potential of the signal T_4, as illustrated in Fig. 6D, which is generated from the CPU 1. As a result, the flip-flop 16 generates a signal T_5, as illustrated in Fig. 6E. Further, by the rise of the potential of the signal $\overline{T_1}$ as illustrated in Fig. 6B, the flip-flop 17 takes in the signal T_5, and, accordingly, the flip-flop 17 generates a signal T_6, as illustrated in Fig. 6F. Therefore, the permission signal T_7 generated from the AND gate 18, which receives the signals T_1 and T_6, is illustrated in Fig. 6G.

During the DMA read or write operation mode, the potential of each of the signals T_4 and T_7 is low and high, respectively. As a result, the gates G_{11} through G_{19} are opened so that the address port 14 accesses the RAM 3 by supplying an externally-applied address signal. In addition, during the DMA read operation mode, the potential of a read/write signal R/W applied to a terminal P_{10} is caused to be high, so as to open the gate G_4 of each port 6-0, 6-1,

..., 6-7. As a result, the ports 6-0, 6-1, ..., 6-7 transmit the DMA data from the RAM 3 to the exterior. In this case, for a time-period wherein the potentials of each of the signals T_4 and T_7 is high and low, respectively, the CPU data is transmitted from the output buffer register 4 through the ports 6-0, 6-1, ..., 6-7 to the exterior. Such two kinds of data, that is, DMA data and CPU data, can be discriminated by the signal T_2 obtained at the terminal P_8, as illustrated in Fig. 6C. In such a DMA read mode, when address signals A, B, ... are supplied to the address port 14, as illustrated in Fig. 6H, DMA read data RA, RB, ... are obtained at the terminal P_0 through P_7, as illustrated in Fig. 6I.

On the other hand, during the DMA write operation mode, the potential of the signal R/W is caused to be low, so as to close the gate G_4 of each port 6-0, 6-1, ..., 6-7. Therefore, write data applied to the terminals P_0, P_1, ..., P_7 is written into an area of the RAM 3 accessed by the address port 14. In this case, as illustrated in Figs. 6H and 6J, write data WA, WB, WC, ... is applied simultaneously with the corresponding address A, B, C, ...

Fig. 7 is a block diagram illustrating a fourth embodiment of the one-chip microcomputer according to the present invention. In Fig. 7, 21 is a register for storing the same data as that of a predetermined area of the RAM 3. That is, when the CPU 1 performs a write operation upon the predetermined area of the RAM 3, the CPU 1 also performs the same write operation upon the register 21. Therefore, the data of the register 21 is always the same as that of the predetermined area of the RAM 3.

During the DMA read operation mode, the DMAC 2, which is set by the CPU 1, transmits the content of the register 21 to a shift register 22.

Next, a shift clock signal generated from a clock generator (not shown) is supplied to the shift register 22 so that the shift operation is performed upon the shift register 22. Therefore, the parallel data stored in the register 21 is converted into serial data which is transmitted through a terminal P_{21} to the exterior.

It should be noted that the above-mentioned predetermined area of the RAM 3 comprises a word (8 bits) allocated by one address. In addition, the predetermined area can comprise at least one predetermined bit of predetermined data words which are, for example, allocated by addresses "0", "1",...,"7".

Figure 8 is a block diagram illustrating a fifth embodiment of the one-chip microcomputer according to the present invention. In Figure 8, an address counter 24 is provided instead of the register 21 of Figure 7. That is, the DMAC 2 increases the address counter 24, so that one word data (8 bits) is read out of the RAM 3 to the shift register 22. Next, a shift clock signal generated from a clock generator (not shown) is supplied to the shift register 22, so that the shift operation is performed on the shift register 22, in the same way as in Figure 7. For example, if the address counter 10 comprises 4 bits, eight words allocated by the addresses "0", "1", "...," "7" can be read out of the RAM 3 to the shift register 22.

In Figures 7 and 8, the DMAC 2 includes some time division means similar to those used in the previous examples to control, via the CPU 1, whether the first data is fed from the serial input/output circuit 23 to the shift register 22 or the second data is fed from the register 21 (or the RAM 3) to the shift register 22.

Note that, in Figures 7 and 8, the DMA operation wherein the data is set in the shift register 22 by the DMAC 2 is never superposed with the CPU operation wherein the shift operation is performed upon the shift register 22.

As explained hereinbefore, the present invention has an advantage in that direct data transfer between the RAM and the exterior can take place without increasing the number of terminals.

C L A I M S

1. A one chip microcomputer comprising:

a central processing unit (CPU 1) having arithmetic, logic and control units;

a random access memory (RAM 3) for storing intermediate data with instructions processed by the central processing unit (CPU 1);

means (4, 23) for carrying first data processed by the central processing unit (CPU 1);

a direct memory access controller (DMAC 2) controlled by the central processing unit (CPU 1) for providing a read out of second data stored in a predetermined area of the random access memory (RAM 3);

means (9, 21) for carrying the second data stored in the predetermined area of the random access memory (RAM 3);

terminal means (P) coupled to said means for carrying the first and second data to provide an output for the first data during a central processing unit operating mode and for the second data during a direct memory access operating mode; and,

a time division means (5) controlled by the direct memory access controller (DMAC 2) for transmitting the first or the second data to the terminal means (P).

2. A one chip microcomputer according to claim 1, in which the means for carrying first data processed by the central processing unit (CPU 1) comprises an output buffer register (OB4) for storing the first data, and in which the means for carrying the second data is a port means (G_1, G_2, G_3) for receiving the first data from the output buffer register (OB4) and the second data from a predetermined area of the random access memory (RAM 3).

3. A one chip microcomputer according to claim 1, in which the means for carrying first data processed by the central processing unit (CPU 1) comprises

an output buffer register (OB 4) for storing the first data, and in which the means for carrying the second data is a gate means (G_{11}, G_{19}) controlled by the central processing unit (CPU 1) an address port means (13) for transmitting an externally applied address signal to the random access memory (RAM 3) under the control of the gate means (G_{11}, G_{19}) so as to read the second data from the random access memory (RAM 3) and port means (G_1) for receiving the first data from the output buffer register (OB4) and the second data from the random access memory (RAM 3) when read by the address port means (10, 11).

4. A one chip microcomputer according to claim 1, in which the means for carrying the first data are formed by a register (21) which is arranged to store the same data as is stored in a predetermined area of the random access memory (RAM 3), the write operation upon the register (21) and upon said predetermined area of the random access memory (RAM 3) being performed simultaneously by the central processing unit (CPU 1), and in which the means for carrying the second data is a parallel-serial converter means (22, 23) controlled by the central processing unit (CPU 1), for converting parallel data into serial data, the parallel data being sent from the register (21) by the direct memory access controller (DMAC 2).

5. A one chip microcomputer according to claim 1, in which the means for carrying the first and second data is a parallel-serial converter means (22, 23) controlled by the central processing unit (CPU 1), for converting parallel data into serial data, and which also includes an address counter (24) controlled by the direct memory access controller (DMAC 2) for generating an address signal to read the second data from the random access memory (RAM 3).

6. A one chip microcomputer according to claim 4 or 5, wherein the parallel-serial converter means comprises:

a shift register (22) for receiving parallel data; and,

a serial input/output circuit (23) controlled by the central processing unit (CPU 1) for performing a shift operation upon the shift register (22).

7. A one-chip microcomputer comprising:

a central processing unit (CPU 1) having arithmetic logic and control units;

a random access memory (RAM 2) for storing intermediate data and instructions processed by the central processing unit (CPU 1);

an output buffer register (OB4) for storing first data processed by the central processing unit (CPU 1);

a direct memory access controller (DMAC 2) controlled by the central processing unit (CPU 1), for reading second data from a predetermined area of the random-access memory (RAM 3);

a port means (G) for receiving the first data from the output buffer (OB 4) and the second data from the random access memory (RAM 3) read by the direct memory access controller (DMAC 2);

terminals (P1-7) connected to the port means (G) and used commonly in both the central processing unit operation mode and the direct memory access mode; and,

a time division means (5) controlled by the direct memory access controller (DMAC 2) for transmitting the first or the second data through the port means (G) to the terminals (P1-7).

8. A one chip microcomputer according to claim 7, further comprising:

an address counter (10) controlled by the direct memory access controller (DMAC 2), for generating an address signal so as to read the second data from the predetermined area of the random access memory (RAM 3).

9. A one chip micorcomputer according to claim 7, further comprising:

a gate means (G_{11}, G_{19}) controlled by the central processing unit (CPU 1);

an address port means (13) for transmitting an externally applied address signal to the random access memory (RAM 3) through the gate means (G_{11}, G_{19}) to read the second data from the random access memory.

10. A microcomputer according to claim 9, wherein the port means (G_{1-5}) comprises bidirectional input/output ports, through which an externally applied data signal is written into an area of the random access memory (RAM 3) accessed by the address port means (13).

11. A one chip microcomputer comprising:

a central processing unit (CPU) having arithmetic, logic and control units;

a random access memory (RAM) for storing intermediate data and instructions processed by said central processing unit;

a register for storing the same data as that of a predetermined area of said random access memory, the write operation upon said register and said predetermined area of said random access memory being simultaneously performed by said central processing unit;

a direct memory access controller (DMAC) controlled by said central processing unit;

a parallel serial converter means, controlled by said central processing unit, for converting parallel data into serial data, said parallel data being sent from said register by said direct memory access controller; and,

a terminal connected to said parallel serial converter means and used commonly for the CPU operation mode and the DMA operation mode.

12. A one chip microcomputer comprising:

a central processing unit (CPU) having arithmetic, logic and control units;

a random access memory (RAM) for storing intermediate data and instructions processed by said central processing unit;

a direct memory access controller (DMAC) controlled by said central processing unit;

an address counter, controlled by said direct memory access controller, for generating an address signal so as to read data from said random access memory;

a parallel serial converter means, controlled by said central processing unit, for converting parallel data into serial data, the data of said random access memory accessed by said address counter being set in said parallel serial converter means;

and,

a terminal connected to said parallel serial converter means and used commonly for the CPU operation mode and the DMA operation mode.

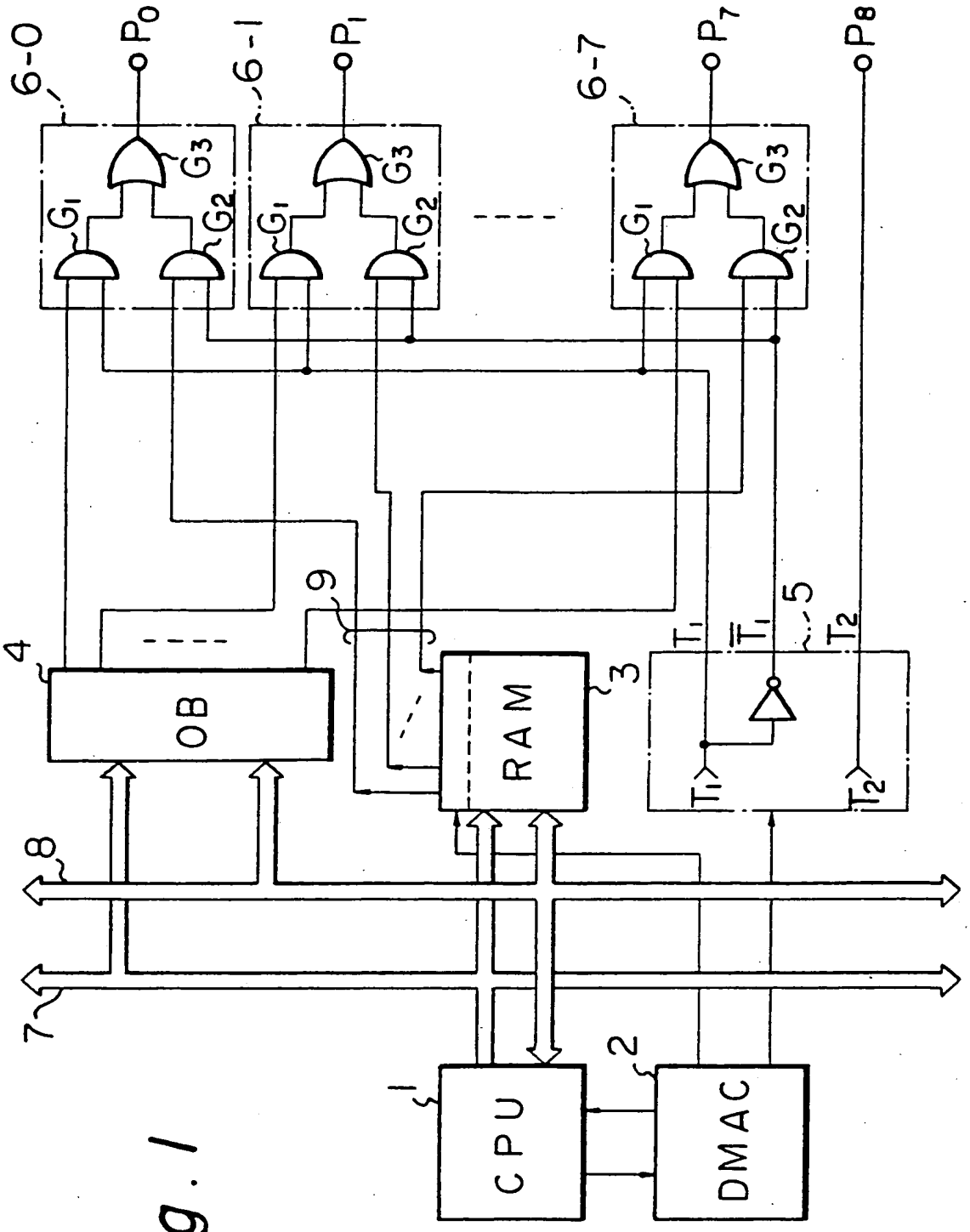


Fig. 1

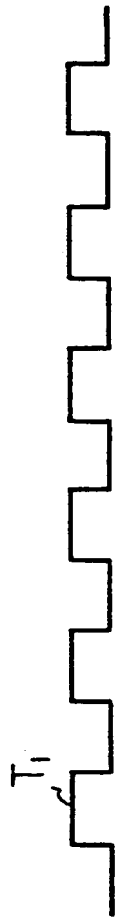


Fig. 2A

Fig. 2B

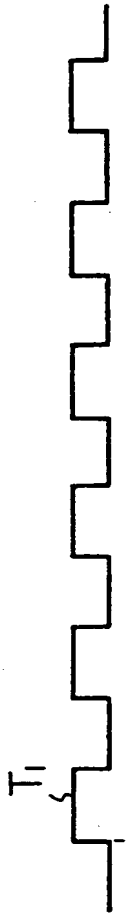


Fig. 4A

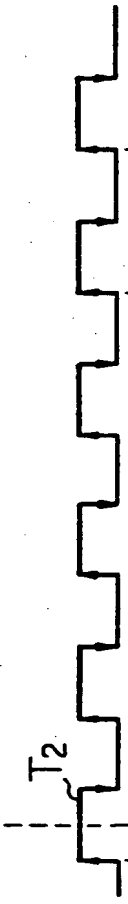


Fig. 4B

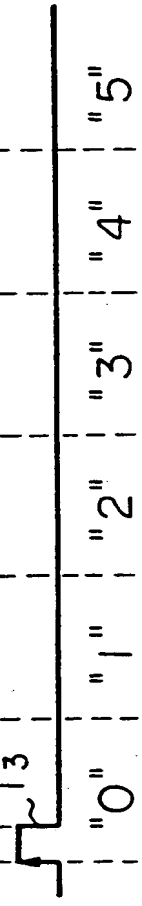


Fig. 4C

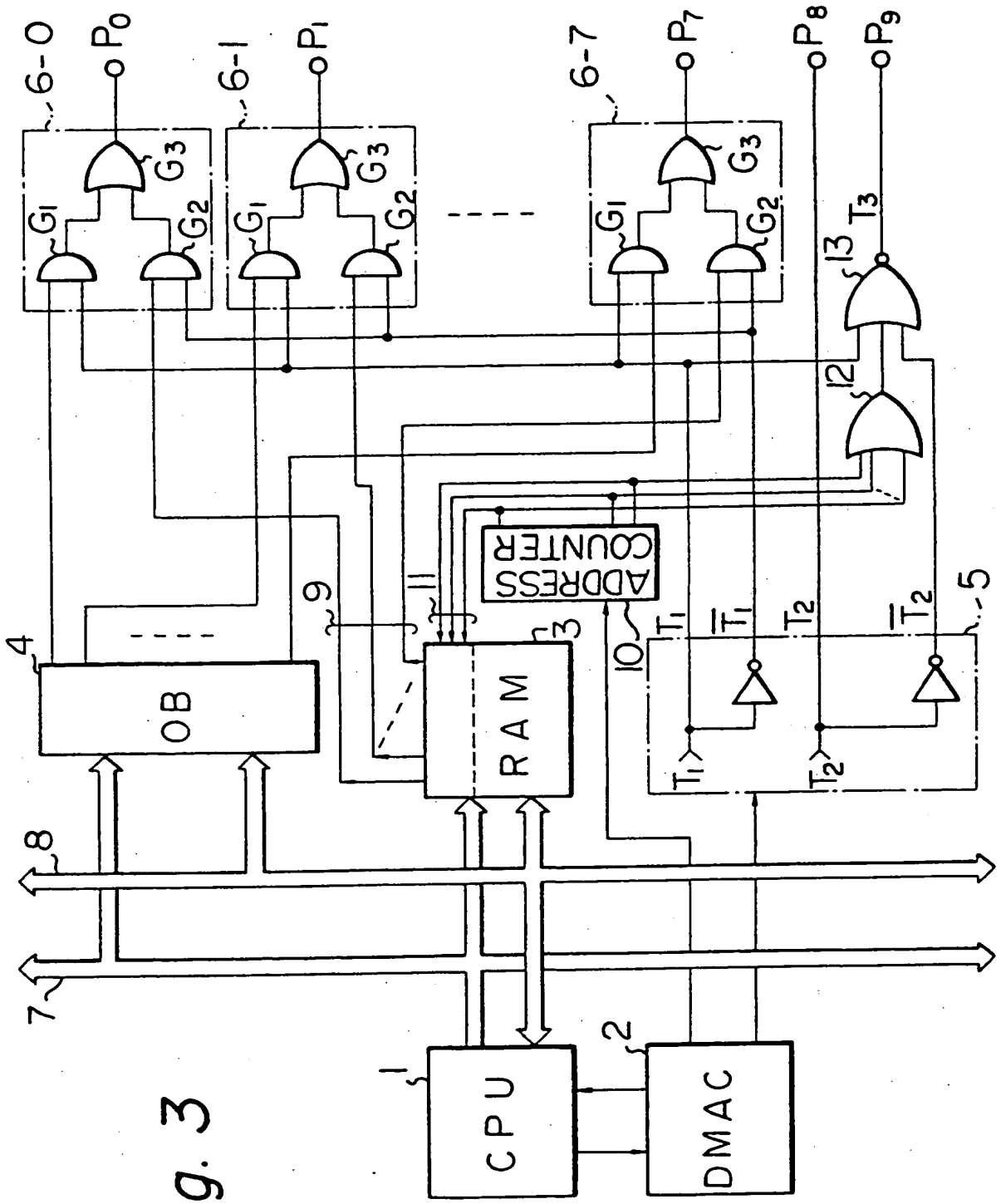
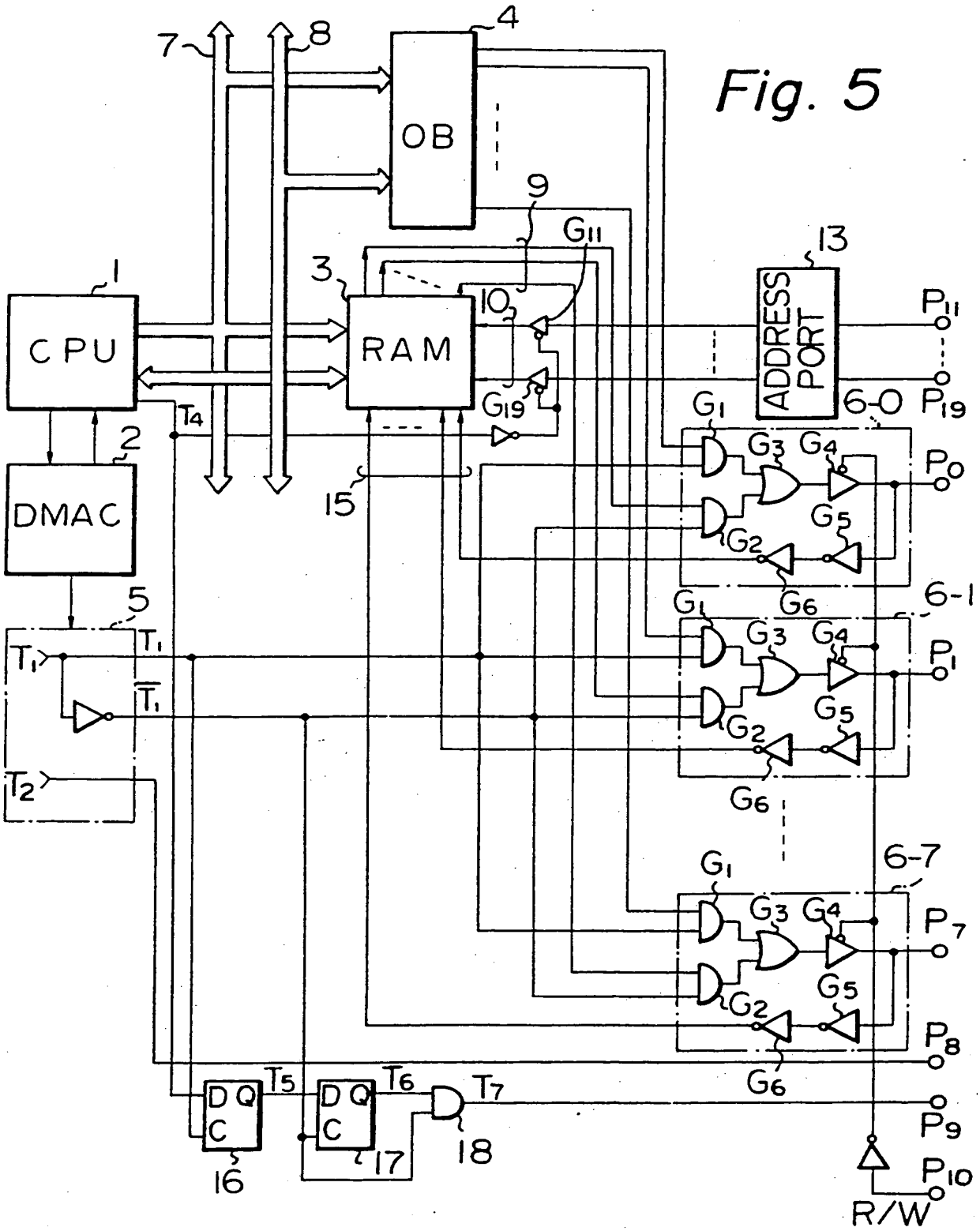

6-0
P0
6-1
P1
6-7
P7
P8
P9
G1
G2
G3
T3
13
12
ADDRESS COUNTER
10
11
9
4
OB
RAM
3
T1
T2
5
8
7
2
1
CPU
DMAC

Fig. 3

0062431

Fig. 5



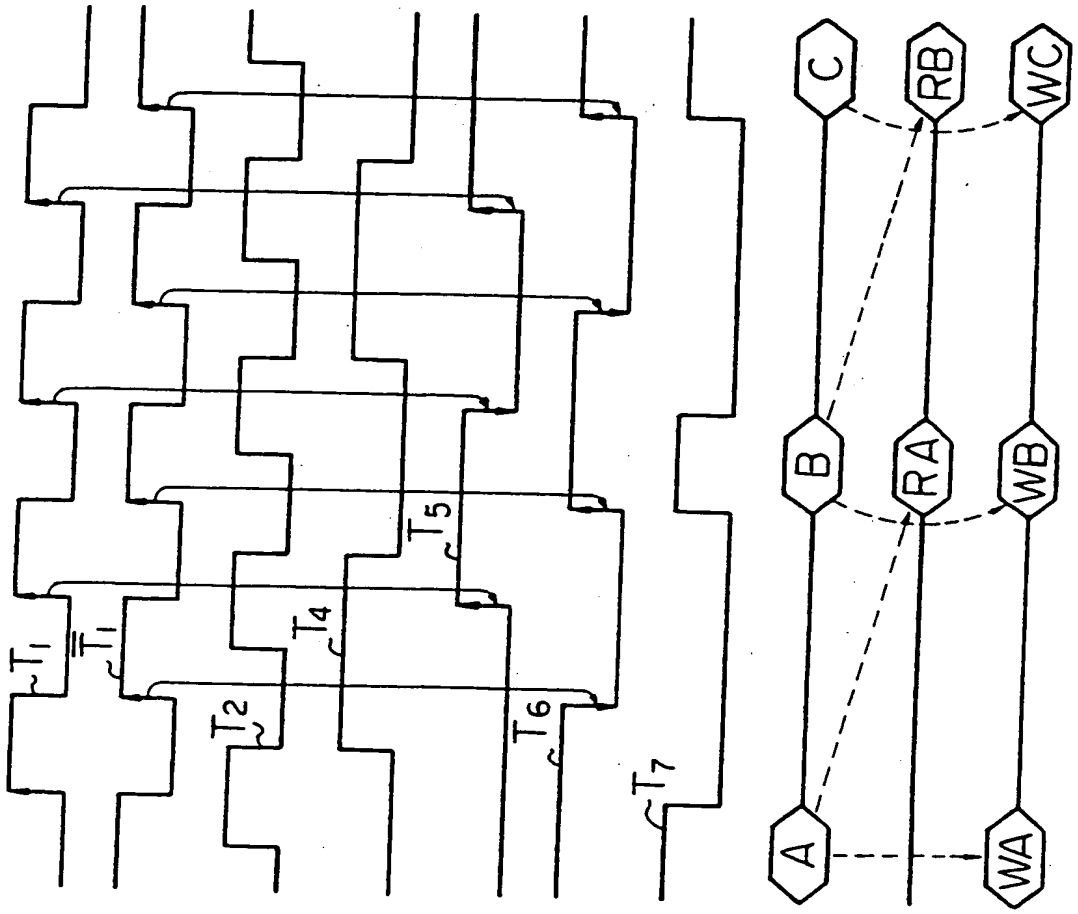


Fig. 6A
Fig. 6B
Fig. 6C
Fig. 6D
Fig. 6E
Fig. 6F
Fig. 6G
Fig. 6H
Fig. 6I
Fig. 6J

Fig. 7

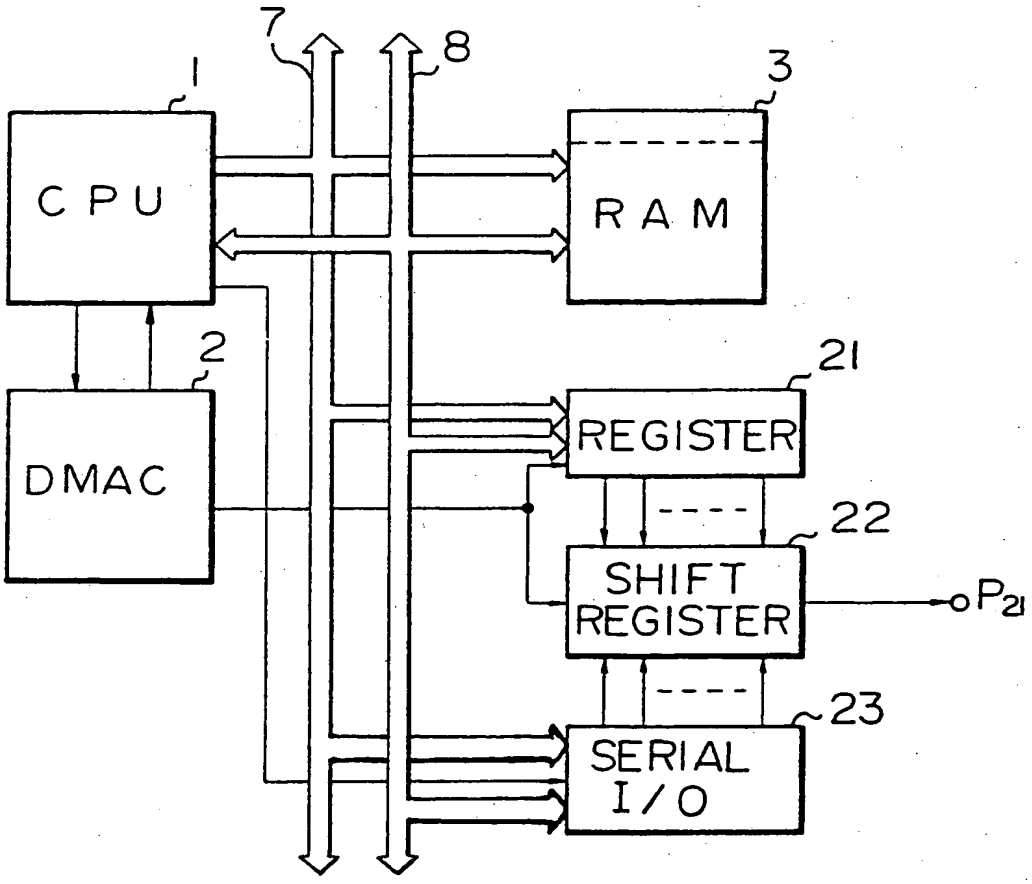
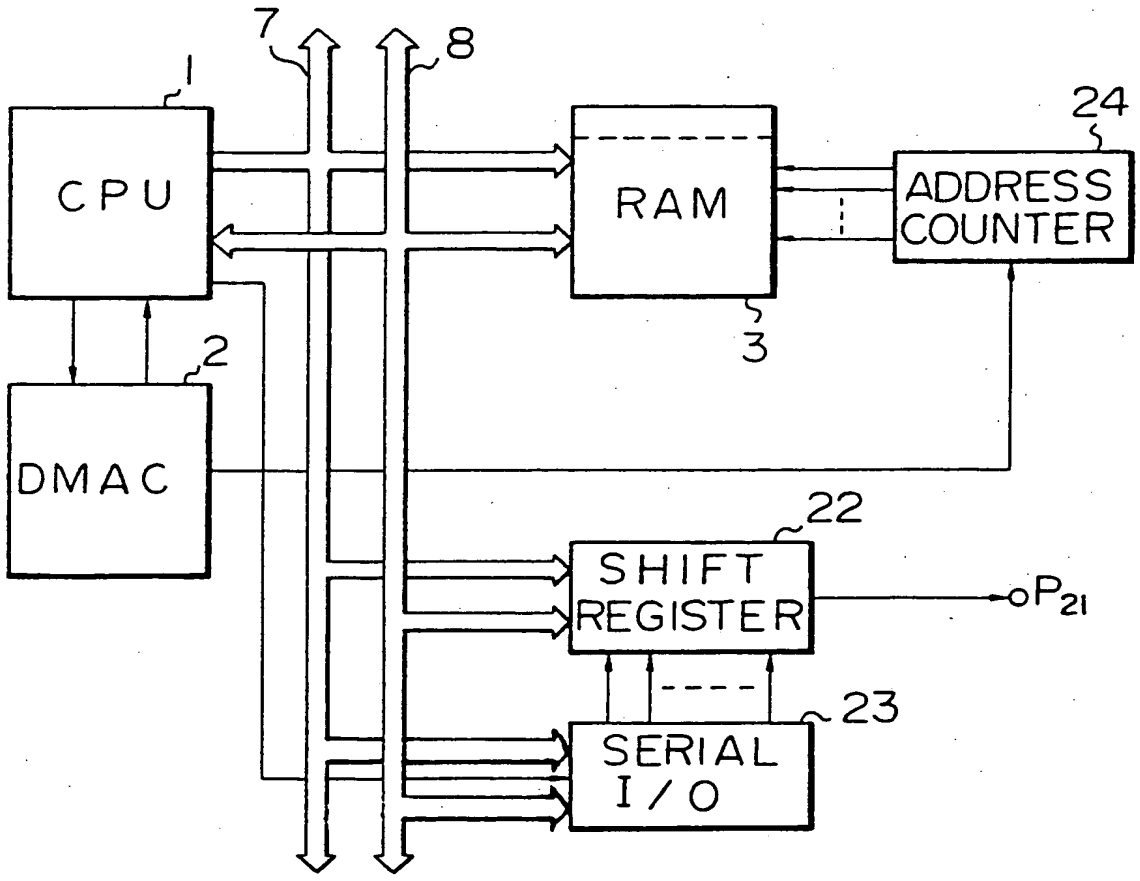

7
8
1
3
CPU
RAM
2
21
DMAC
REGISTER
22
SHIFT
REGISTER
P21
23
SERIAL
I/O

Fig. 8


7
8
1
CPU
RAM
24
ADDRESS
COUNTER
3
2
DMAC
22
SHIFT
REGISTER
P21
23
SERIAL
I/O

European Patent Office

0062431

Application number

EP 82 30 1445

EUROPEAN SEARCH REPORT

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
Y	US-A-4 240 138 (TEXAS INSTRUMENTS) *Column 1, lines 40-60; column 2, lines 18-56; column 3, lines 12-45; column 6, lines 25-30; figures 1-4*	1,2,3, 7	G 06 F 3/04 G 06 F 15/06
Y	IEEE DIGEST OF PAPERS FTCS-10, 1st-3rd October 1980, The 10th international symposium on fault - tolerant computing Kyoto, Japan, New York (USA); S.FUNATSU et al.: "Digital fault simulation in bidirectional bus circuit environments" *Page 155, column 1, lines 14-23; column 2, lines 6-24; figures 1,2*	1,7,10	
Y	DE-A-2 045 833 (SHARP) *Page 1, lines 1-5; page 4, lines 9-25; page 7, lines 1-7; page 8, lines 2-20; figures 1,2*	1,7	TECHNICAL FIELDS SEARCHED (Int. Cl. ³) G 06 F 3/04 G 06 F 15/06
Y	ELECTRONIC DESIGN, vol. 26, no. 13, June 1978, pages 78-84, Rochelle Park (USA); BURTON: "Know a microcomputer'S bus structure". *Figure 3, page 79; page 80, first column, lines 20-37; figure 6, page 81*	1,7,10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	02-07-1982	DHEERE R.F.B.M.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503 03 82

European Patent Office

EUROPEAN SEARCH REPORT

0062431
Application number

EP 82 30 1445

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	ELEKTRIE, vol. 32, no. 8, 1978, pages 429-437, Berlin (DE); M.HANN et al.: "Mikroprozessoren, Mikroprozessrechner und Mikroprozessrechnersysteme". *Page 429, second column, lines 64-72; page 430, first column, lines 1-3; figure 2; page 431, second column, lines 6-13; figure 6*	4-6,11,12	
A	THE BELL SYSTEM TECHNICAL JOURNAL, vol. 58, no. 4, April 1979, pages 959-962, New York (USA); W.F.CHOW et al.: "MAC-4: A single-chip microcomputer".	1	
A	US-A-4 181 938 (TOKYO SHIBAURA)	1	TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	02-07-1982	DHEERE R.F.B.M.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503. 03.82